# RTL DESIGN OF RUN- LENGTH ENCODING USING VERILOG HDL

#### Flora Das<sup>1</sup>

Department of Electronics and Communication, Aryan Institute of Engineering and Technology Bhubnaeswar **Sambhunath Biswas**<sup>2</sup> Department of Electronics and Communication, Raajdhani Engineering College, Bhubaneswar **Smruti Samantray**<sup>3</sup> Department of Electronics and Communication,

Capital Engineering College (CEC), Bhubaneswar Supriya Nayak<sup>4</sup>

Department of Electronics and Communication, NM Institute Of Engineering & Technology, Bhubaneswar

#### ABSTRACT

Compression is an efficient technique to reduce the memory size and to improve the speed. In ECG signal compression, modified run-length encoding plays a significant role to compress the digitized ECG signals. The main objective of this paper is to realize an efficient architecture for modified run-length encoding compression and decompression algorithms. The proposed architectures designed in verilog HDL. And the designed verilog HDL modules are simulated and synthesized using Xilinx ISE 13.1 for RTL design.

**Key words:** Modified Run-Length Encoding; Compression; Decompression; Verilog HDL; RTL Design.

# **1. INTRODUCTION**

In modern Bio-medical signal processing, the storage, processing and transmission of large quantities of digitized ECG signals for reproductive purpose is required. Data compression is needed to reduce the space required to store and transmit digitized ECG signals [1]. In discrete wavelet transform based ECG signal compression alorithm, firstly the ECG signals are decomposed by using forward discrete wavelet transformation. Secondly the thresholding will be done for the decomposed signals. Next modified runlength encoding and decoding is done to compress and decompress the digitisized signals. Lastly the reconstruction will be done by using inverse discrete wavelet transformation.

Compression can be done in two ways- lossless compression and lossy compression. Lossless compression is a class of data compression algorithm that allows the original data to be perfectly reconstructed from the compressed data. The original data and the data after compression and decompression are exactly the same because no part of the data is lost in the process [2]. Lossy compression discards the partial data to represent the content. This is used to reduce data size for storage, handling and transmitting content. In most cases a lossy method can produce a much smaller compared file than any lossless method, while still meeting the requirements of the applications. Lossy methods are most often used for compressing sound, images or videos.

In this paper, lossy data compression is used to design efficient modified run-length encoding compression and decompression architectures using verilog HDL. And the designed modules are simulated and synthesized using Xilinx ISE 13.1.

# 2. RUN LENGTH ENCODING

Run length encoding algorithm uses lossless data compression technique. In the run length encoding the runs (identical data) of data are stored as a single value and count, rather than as the original data. For example, if the input sequence is 44, 44, 44, 45, 45, 27, 27, 26, 26 then the output sequence will be (44, 4), (45, 2), (27, 2), (26, 2). From the above example it is clear that, the compression ratio is better for the longer runs of data.

# **3. EFFICIENT MODIFIED RUN LENGTH ENCODING**

### Compression

The efficient modified run length encoding compression algorithm uses lossy compression technique. With this lossy compression, the compression ratio can be improved, which causes to improve the system performance as well. In this technique, first input data is printed at the output. If the next input data is equal to or 1 bit greater than or 1 bit less than the previous data, then this data is considered in the run and count is incremented. If the modified run length encoding algorithm is applied to the same example mentioned above, 44, 44, 44, 45, 45, 27, 27, 26, 26 then instead of (44, 4), (45, 2), (27, 2), (26, 2), the output sequence will be (44, 6), (27,4). From the example it is known that the compression ratio is improved when compared to run length encoding.

The flow chart of compression algorithm is given in figure 1.



Figure 1

The algorithm for modified run-length encoding compression algorithm is described below.

- Read first data from the input sequence.
- Print first data.
- Print count=1.
- Read next data.
- If next data=first data or first data+1 or first data-1 then go to step 6. Otherwise go to step 8.
- Print count=count+1.
- Go to step 4.
- Print next data.
- Go to step 3.

Figure 2 shows the architecture of modified run-length encoding compression algorithm.



Figure 2

### Decompression

The flow chart of decompression algorithm is given in figure 3.



Figure 3

The algorithm for modified run-length encoding compression algorithm is described below.

- Read input data and count.
- Print input data.
- Count=count-1.
- If count=1 then go to step 1. Otherwise go to step 2.

Figure 4 shows the architecture of modified run-length encoding compression algorithm.



Figure 4

### 4. RESULTS

The modified run-length encoding compression and decompression architectures are designed using Verilog HDL. The designed modules are simulated and synthesized using Xilinx ISE 13.1. and figure 8 shows the RTL schematic of decompression algorithm.

The output waveform of modified run-length encoding compression module is shown in figure 5.

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Figure 5

The output waveform of modified run-length encoding decompression module is shown in figure 6.



#### Figure 6

Figure 7 shows the RTL schematic of modified run-length encoding compression architecture.



#### Figure 7

Figure 8 shows the RTL schematic of modified run-length encoding decompression architecture.



Figure 8

# **5. CONCLUSION**

In this paper, Lossy data compression is used to design efficient modified run-length encoding compression and decompression architectures using verilog HDL. And the designed modules are simulated and synthesized using Xilinx ISE 13.1. The given input sequence is encoded using compression algorithm. And decompression algorithm is applied to the compressed data to get the original sequence. Lossy data compression is used to compress the data. By using these architectures, the efficient compression rate is achieved.

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